

FIG. 1A

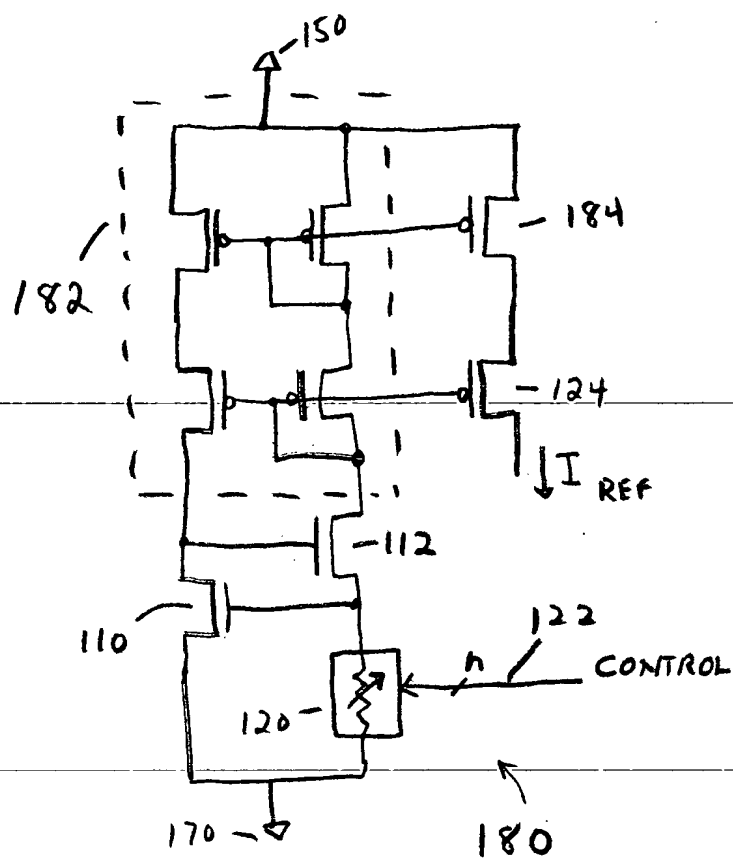


FIG. 1B

FIG. 2 is a schematic diagram of a circuit for a memory array, showing a series of memory cells connected to a common data line.

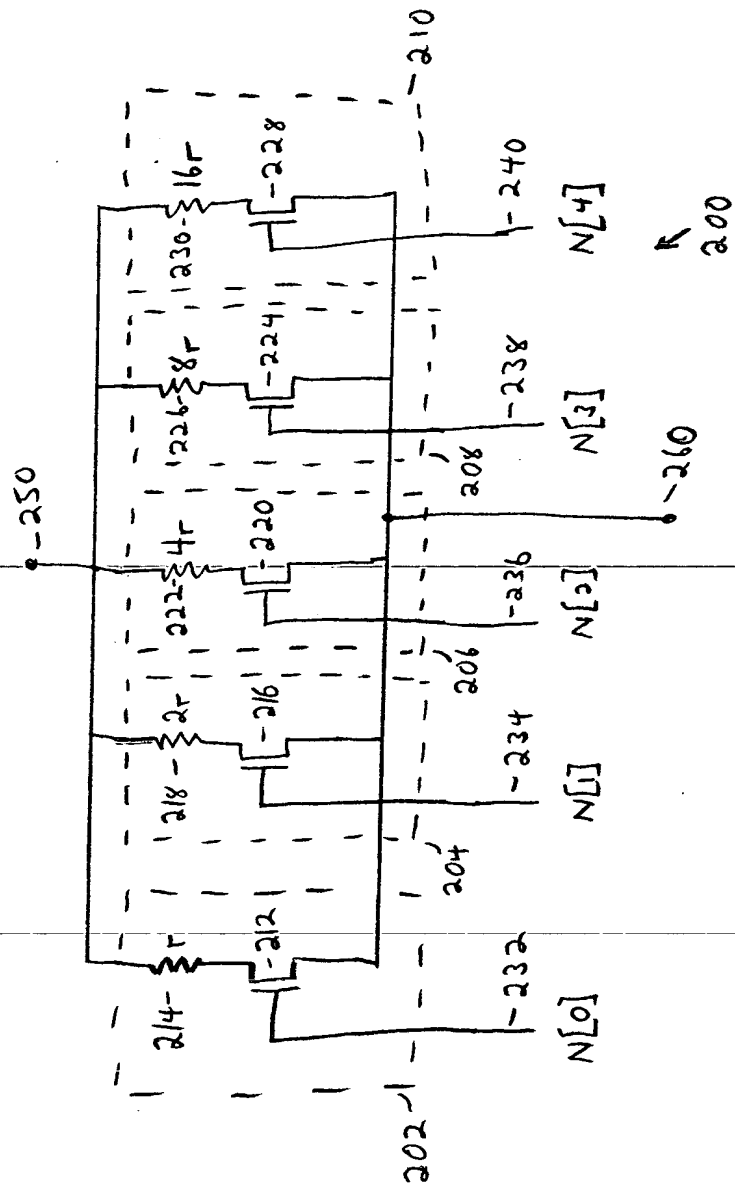


FIG. 2

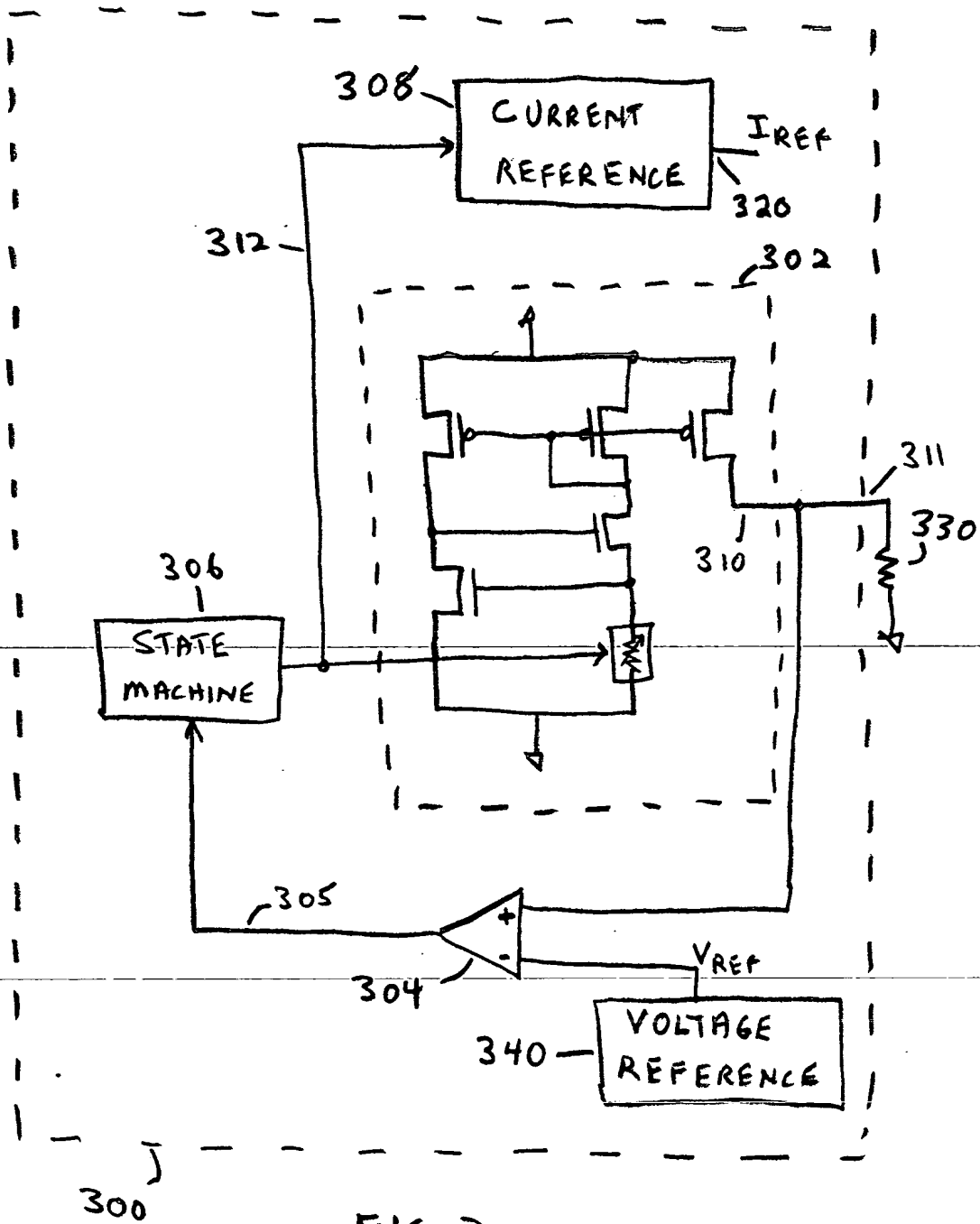


FIG. 3

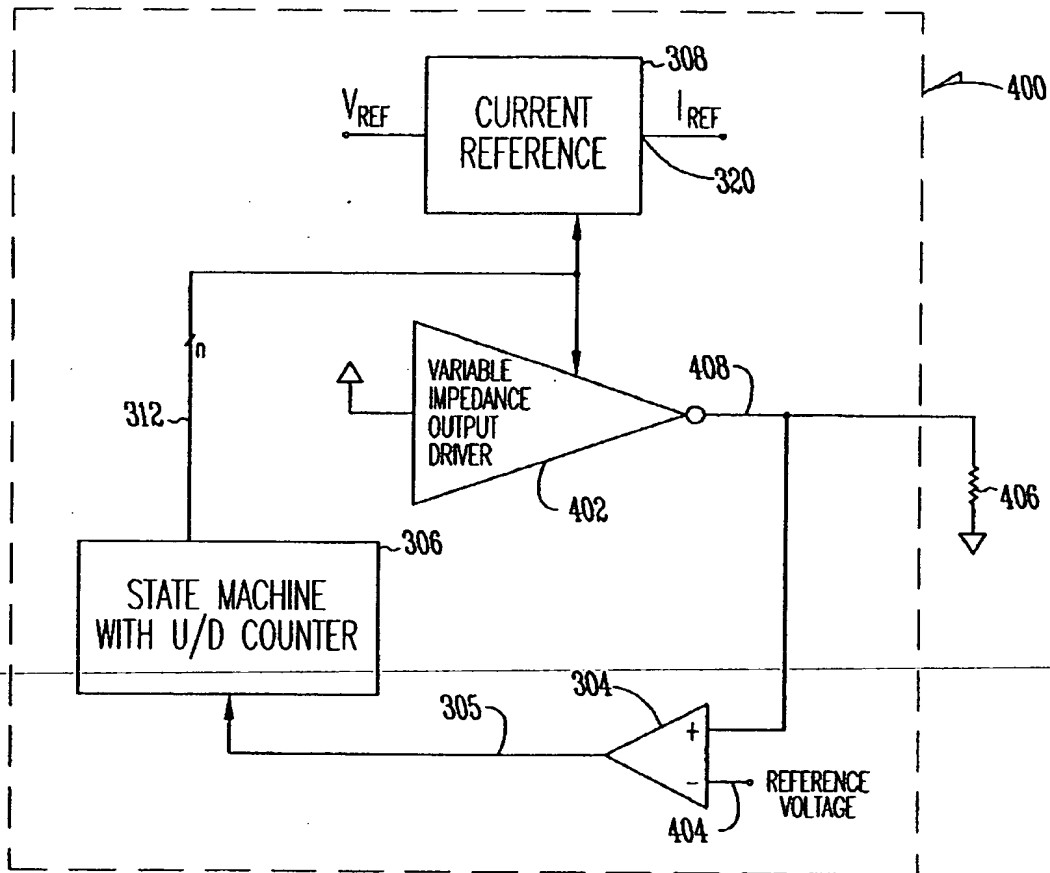


Fig. 4

6/16

0000503 44504

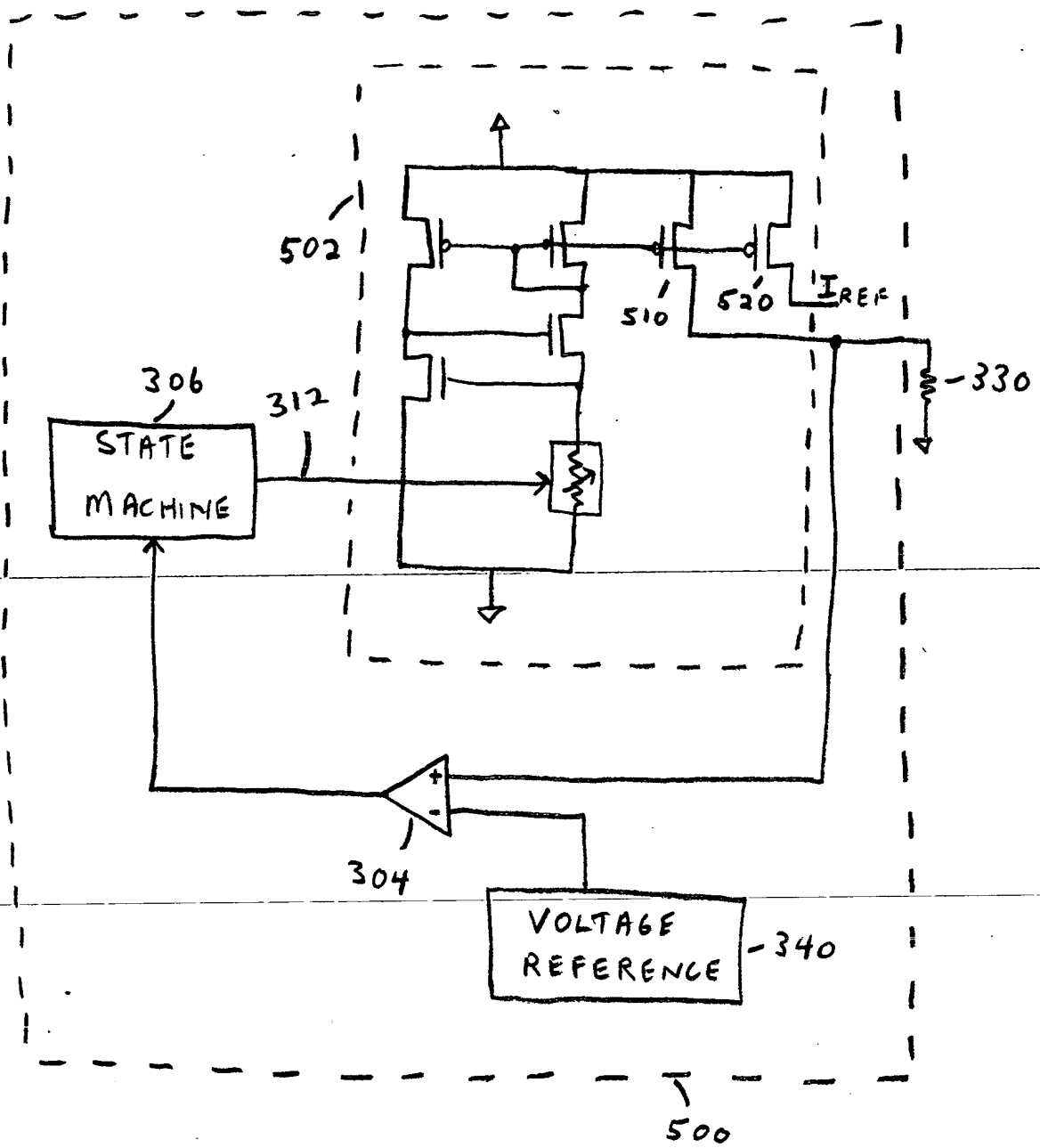


FIG. 5